In The Claims:

Please amend the claims as follows:

Claim 1. (currently amended) A graphics display method for continuously displaying a plurality of graphics data on multiple display devices of a computer system that contains a central processing unit (CPU) which has a memory controller inside, a graphics-processing unit coupled to the memory controller, and a system memory directly accessed by [[a]]the CPU, wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and using [[a]]the common clock source to synchronize a plurality of blank periods of the display devices;

receiving a power saving signal from the CPU, [[said]]the power saving signal indicates a request for executing a power saving process by the CPU during a[[n]] non-responding period of the CPU, so as to reduce power consumption of the CPU, wherein memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU; and

executing the power saving process within [[the]]a least common multiple occurrence of the blank periods of the display devices.

Claim 2. (currently amended) The method of claim 1, further comprising a step of detecting the upcoming least common multiple occurrence of the blank periods of the display devices before [[the]] executing [[step]]the power saving process.

Claim 3. (currently amended) The method of claim 1, wherein the blank periods can be a plurality of horizontal blank periods (HBPs) or a plurality of vertical blank periods (VBPs).

Claim 4. (currently amended) The method of claim 3, wherein the horizontal blank periods or the vertical blank periods [[is]]are provided by [[a]]the graphics-processing unit.

Claims 5-16 (cancelled)

Claim 17. (currently amended) A graphics display method for continuously displaying a plurality of graphics data on multiple display devices of a computer system that contains a central processing unit (CPU) which has a memory controller inside, a graphics-processing unit coupled to the memory controller, and a system memory directly accessed by [[a]]the CPU, wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and using [[a]]the common clock source to synchronize blank periods of the display devices;

receiving a power saving signal from the CPU, [[said]]the power saving signal indicates a request for executing a power saving process [[by]]to make the CPU self-adjust ~~self-adjusting~~ a CPU ~~frequency~~ clock rate and a power level of the CPU during a[[n]] non-responding period of the CPU, wherein memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU; and

executing the power saving process within [[the]]a least common multiple occurrence of the blank periods of the display devices.

Claim 18. (currently amended) The method of claim 17, wherein while executing the power saving process, the system memory is continuously accessed by the CPU during the non-responding period of the CPU.

In The Drawings:

Please substitute the attached clean sheets of drawings of Figs. 3 and 4 for the original drawings of Figs. 3 and 4. Compared with the original FIG. 3, the reference characters "32", "33", "35", "36", "37", "39", and "40" are cancelled in the amended FIG.. 3. Compared with the original FIG. 4, the reference characters "37", "39", "40", "42", "43", "45", and "50" are cancelled in the amended FIG. 4.